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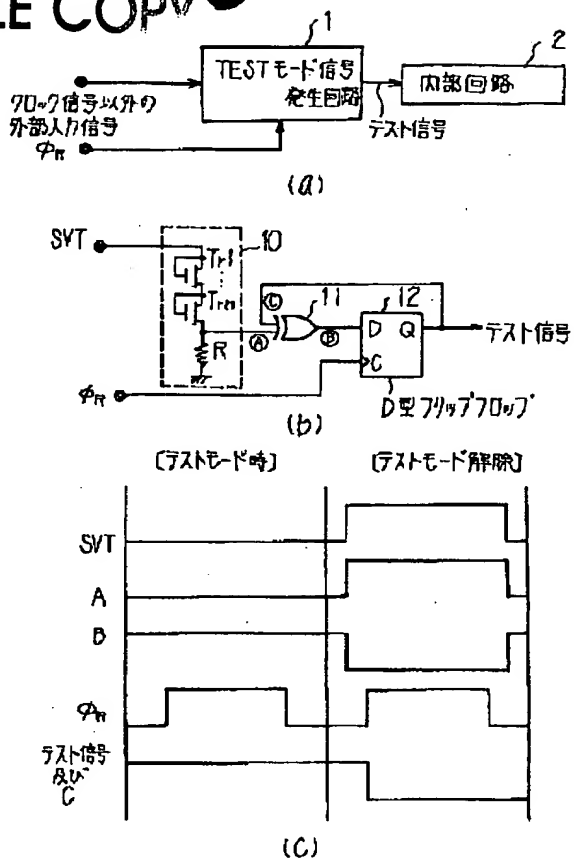
TITLE : TEST MODE SIGNAL GENERATION CIRCUIT OF SEMICONDUCTOR DEVICE



ABSTRACT : PURPOSE: To reduce a malfunction due to a test mode release irrespective of the intentional release of the test mode when an unexpectable change in a pulse width is generated due to fluctuation, noise or the like of internal waveform in a used tester in the test mode.

CONSTITUTION: A test mode signal generation circuit is provided with an input circuit 10, with an exclusive-OR (Ex-OR) circuit 11 and with a D-type flip-flop(DFF) circuit 12. The output terminal of the input circuit 10 is connected to the input terminal, on one side, of the Ex-OR circuit 11, and its output terminal is connected to the data-signal input terminal D of the DFF circuit 12. A clock φR is supplied to the clock signal input terminal C of the DFF circuit 12, and its output terminal Q is connected to the input terminal, on the other side, of the Ex-OR circuit 11. In a test mode, a high level is input as an output signal TEST, and a low level is output when the test mode is released.